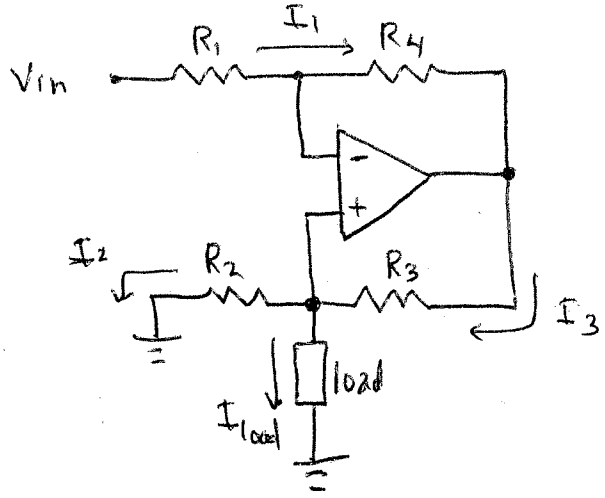
PHYS 220 Physical Electronics Problem Set #5 SOLUTIONS

H+H 4.2, 4.3, additional exercise #2

8.5, 8.7, 8.8, 8.9

4.2 The Howland Current Source.



Since the op amp keeps its inputs at the same potential, the voltage across R_4 equals the voltage across R_3

$$-I_3R_3 = I_1R_4 \qquad (1)$$

↑ to be consistent with directions shown on diagram

Since no current flows into or out of the op-amp inputs (and charge is conserved)

$$I_3 = I_2 + I_{load} \qquad (2)$$

Putting (2) into (1) $\Rightarrow$ $\quad I_2R_3 + I_{load}R_3 = -I_1R_4$

or... $\quad I_{load} = -I_1\left(\frac{R_4}{R_3}\right) - I_2$

Now $I_2 = \frac{V_+}{R_2} = \frac{V_-}{R_2}$ since $V_+ = V_-$

and... $V_- = V_{in} - I_1 R_1$ so...

$$I_{load} = -I_1\left(\frac{R_4}{R_3}\right) - \frac{V_{in}}{R_2} + I_1\frac{R_1}{R_2}$$

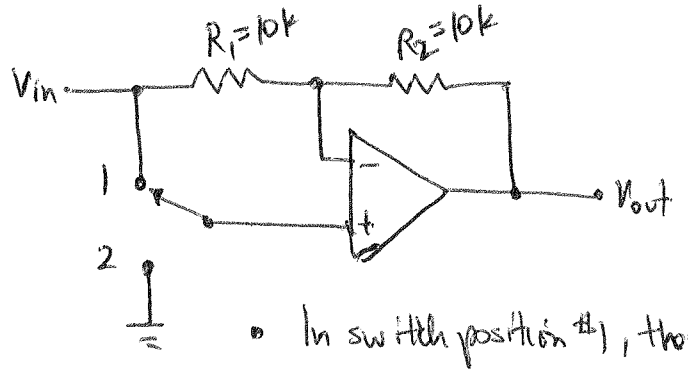
or.. $$I_{load} = -\frac{V_{in}}{R_2} + I_1\underbrace{\left[\frac{R_1}{R_2} - \frac{R_4}{R_3}\right]}_{\text{set this to zero...}}$$

choosing $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ or $\frac{R_3}{R_2} = \frac{R_4}{R_1}$, then

$$\boxed{I_{load} = -\frac{V_{in}}{R_2}}$$ as indicated on p. 182.

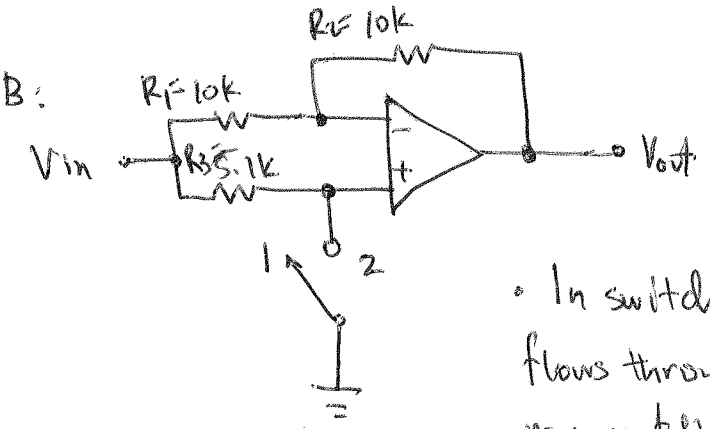
4.3 Analyze the "optional* inverter" circuits of Fig. 4.14.

A:



- In switch position #1, there is no voltage across the 1st resistor (since $V_+ = V_-$), so no current flows through it. Therefore no current flows through the second resistor either and $V_{out} = V_- = V_+ = V_{in}$ ∴ unity-gain follower.
- In switch position #2, we have an inverting amplifier (see Fig. 4.4) with gain $= -\frac{R_2}{R_1} = -1$.

B:



- In switch position #1, no current flows through R_3 (5.1kΩ) since no current flows into an op-amp input.

Therefore $V_+ = V_{in} = V_-$.

No voltage appears across R_1, so no current flows in R_1 or R_2 ... $V_{out} = V_- = V_+ = V_{in}$

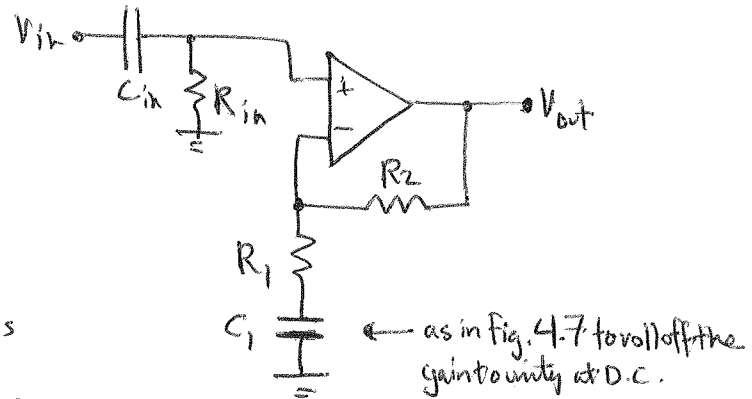
⇒ unity gain follower.

- In switch position #2. $V_+ = 0$, so we have our ordinary inverting amplifier ... (V_- is a virtual ground) with gain $= -\frac{R_2}{R_1} = -1$

Note that some current flows through R_3 (5.1kΩ) to ground so the input resistance is the parallel combination of R_1 and R_3.

Ch.4 Additional Exercise #2: Design a capacitively coupled, non-inverting audio amplifier using an op-amp with gain = 20 dB, Z_{in} = 10k, and the −3dB point at 20 Hz

See fig. 4.6 on p. 179



20 dB gain ⇒ $A_V = 10$

on p. 178, we find

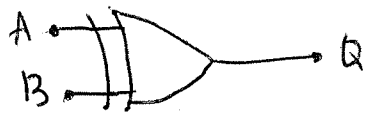
$A_V = 1 + \frac{R_2}{R_1}$ for this configuration so ... $\frac{R_2}{R_1} = 9$ ... may choose $R_1 = 2.0k$ and $R_2 = 18k$ as in Fig. 4.6

To get $Z_{in} = 10k$ in the passband ... choose $R_{in} = 10k$

To get $f_{3dB} = 20Hz$, choose C_{in} such that $\frac{1}{2\pi R_{in} C_{in}} = 20Hz$ or $C_{in} = 0.8\mu F$

and choose C_1 such that $\frac{1}{2\pi R_1 C_1} = 20Hz$ $C_1 = 4\mu F$

8.5 Use an exclusive-OR gate as an optional inverter



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Use B as the control ... if B=0 then...

A	Q
0	0
1	1

and the gate acts as a buffer without inversion

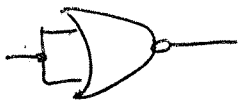
if B=1 then

A	Q
0	1
1	0

and the gate acts as an inverter.

8.7 What do the circuits in Fig. 8.12 do?

A:



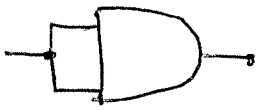
NOR Gate Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

A	Q
0	1
1	0

This is an inverter!

B.



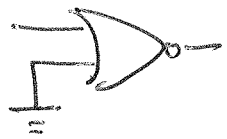
AND Truth Table

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

A	Q
0	0
1	1

This is a buffer!

c.



NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

B LOW

A	Q
0	1
1	0

This is also an inverter!

D.

NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

B	Q
0	0
1	0

Always returns a Low output.

E.

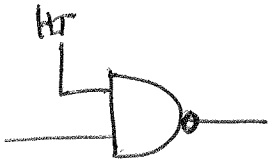
AND

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

A	Q
0	0
1	0

Always returns a Low output.

F.



NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

B	Q
0	1
1	0

This is an inverter.

8.8 Using 2-input gates show how to make

(a) INVERT from NOR ... see 8.7 part A or part C

(b) OR from NORs ...

OR = NOT NOR so ...

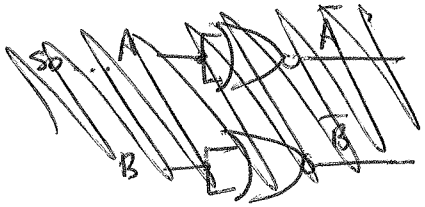
(c) OR from NANDs ...

NAND $\Rightarrow$ $\overline{A \cdot B} = \bar{A} + \bar{B}$ by DeMorgan's Thm.

or starting both $A+B = \overline{\overline{A+B}} = \overline{\bar{A} \cdot \bar{B}}$

A OR B = NOT (NOT A and NOT B)

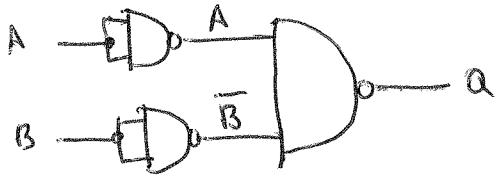
NAND (NOT A, NOT B)



Note that a NAND gate with both inputs connected together is an inverter

NAND A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

so ...

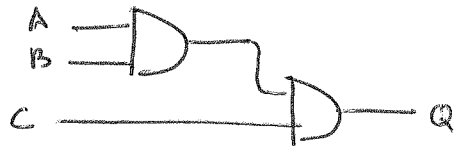


$Q = \overline{\bar{A} \cdot \bar{B}} = A + B$

8.9 (a) Make a 3-input AND gate from 2-input ANDs..

Note that $A \cdot B \cdot C = (A \cdot B) \cdot C = A \cdot (B \cdot C)$
(see p. 491, table 8.3)

So..

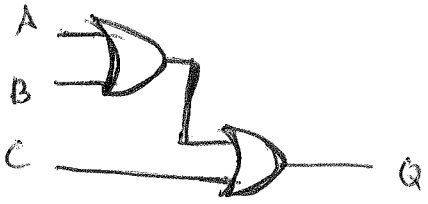


A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b) Make a 3-input OR gate from 2-input ORs

Note that $A+B+C = (A+B)+C = A+(B+C)$
(see p. 491, table 8.3)

So..



A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(c) Make a 3-input AND from 2-input NANDs

Since we can make INVERTERS out of NANDs...